ABSTRACT OF THE DISCLOSURE

A Local Area Network based on a parallel bus architecture is disclosed. The LAN provides a means of utilizing relatively low cost CMOS circuitry to obtain performance superior to LAN's utilizing more exotic high speed technology. The disclosed LAN is based on a parallel bus having nx8 data lines, ± power lines, and a clock line. The bandwidth of the LAN is the product of the number of data lines times the clock speed. Bandwidth is therefore scalable by increasing either the clock speed, the number of data lines, or both. Access to the bus is provided via ports which include transceivers, a clock receiver, and a configurable hardware interface. Each port is assigned an address based on a data line and a clock cycle. The invention features a network that becomes more efficient as usage increases, ports that can accept any medium, and an architecture that facilitates implementation of a true ``STAR'' LAN configuration which interfaces between two or more serial communications links.